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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/687,453	10/13/2000	James M. Van Dyke	18659-23	1345

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EXAMINER
CHEN, CHONGSHAN

ART UNIT	PAPER NUMBER
2172	9

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/687,453	VAN DYKE ET AL.	
	Examiner	Art Unit	
	Chongshan Chen	2172	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This action is responsive to communications: Amendment A, filed on 4/2/03. This action is made final. Claims 1-21 are cancelled, and claims 32-67 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 32-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (5,500,939).

As per claim 32, Kurihara discloses a graphics system, comprising:

a graphics memory (Kurihara, Fig. 1, 2 Memory);

a graphics memory access bus connected to said graphics memory (Kurihara, Fig. 1);

a plurality of graphics processing units (Kurihara, Fig. 1, 6, Graphic Processor); and

a memory controller connected between said graphics memory access bus and said plurality of graphics processing units, dividing said graphics memory access bus into individual bus partitions, each of which is a fraction of the graphics memory access bus size, said memory controller partitioning information within said graphics memory into independently accessible memory partitions, said memory controller routing data from said independently accessible memory partitions to said plurality of graphics processing units via said individual bus partitions (Kurihara, Fig. 1, col. 3, lines 5-40).

Kurihara does not explicitly disclose memory controller providing a non-partitioned view of said graphics memory to said plurality of graphics processing units. However, the graphic controller selects individual processor without user intervention (Kurihara, col. 4, lines 13-21). The user does not need to know which process and partition is selected because the graphic controller handles all the work. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a non-partitioned view of said graphics memory because the user does not need to know how the memory is partitioned. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a non-partitioned view of said graphics memory because the user does not need to know how the memory is partitioned.

As per claim 33, Kurihara teaches all the claimed subject matters as discussed in claim 32, and further discloses memory controller includes control logic to select one or more of said individual bus partitions to route data in response to a data request from a graphics processing unit of said plurality of graphics processing units (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 34, Kurihara teaches all the claimed subject matters as discussed in claim 32, and further discloses memory controller maps data to said independently accessible memory partitions in an interleaved fashion to balance memory load across said independently accessible memory partitions (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 35, Kurihara teaches all the claimed subject matters as discussed in claim 32, and further discloses individual bus partitions have corresponding individual queues (Kurihara, Fig. 1).

As per claim 36, Kurihara teaches all the claimed subject matters as discussed in claim 35, except for explicitly disclosing a multiplexer to combine data from said individual queues. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a multiplexer to combine data from individual queues in order to combine data. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a multiplexer to combine data from individual queues in order to combine data.

As per claim 37, Kurihara teaches all the claimed subject matters as discussed in claim 35, except for explicitly disclosing individual queues have corresponding arbiter circuits. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have individual queues with corresponding arbiter circuits in order to accept bus requests from requester modules and grants control of the data transfer bus to one requester at a time. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have individual queues with corresponding arbiter circuits in order to accept bus requests from requester modules and grants control of the data transfer bus to one requester at a time.

As per claim 38, Kurihara teaches all the claimed subject matters as discussed in claim 35, and further discloses individual queues facilitate ordered read data delivery and thereby prevent deadlocking across said individual bus partitions (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 39, Kurihara teaches all the claimed subject matters as discussed in claim 38, and further discloses individual queues process read data requests that span a plurality of individual bus partitions (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 40, Kurihara teaches all the claimed subject matters as discussed in claim 37, and further discloses prioritize requests from a sub-set of said plurality of graphics processing units (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 41, Kurihara teaches all the claimed subject matters as discussed in claim 40, and further discloses sub-set of said plurality of graphics processing units share a command and write data path (Kurihara, Fig. 1).

As per claim 42, Kurihara teaches all the claimed subject matters as discussed in claim 40, except for explicitly disclosing graphics processing unit of said sub-set of said plurality of graphics processing units has a sub-request ID. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include request ID in order to identify request. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include request ID in order to identify request.

As per claim 43, Kurihara teaches all the claimed subject matters as discussed in claim 40, and further discloses arbiter circuit pre-arbitrates requests from a sub-set of low-bandwidth graphics processing units (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 44, Kurihara teaches all the claimed subject matters as discussed in claim 43, and further discloses arbiter circuit treats said sub-set of lowbandwidth graphics processing units as a single client (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 45, Kurihara teaches all the claimed subject matters as discussed in claim 32, and further discloses individual memory partitions of said independently accessible memory partitions are assigned to solely service individual graphics processing units of said plurality of graphics processing units (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 46, Kurihara teaches all the claimed subject matters as discussed in claim 32, and further discloses a selected graphics processing unit of said plurality of graphics processing units accepts data in an out-of-order fashion (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 47, Kurihara teaches all the claimed subject matters as discussed in claim 46, and further discloses graphics processing unit accepts data as soon as said data is available from a partition (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 48, Kurihara teaches all the claimed subject matters as discussed in claim 35, and further discloses individual queues include request queues and read data return queues to balance data locality requirements to facilitate memory access efficiency (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 49, Kurihara teaches all the claimed subject matters as discussed in claim 37, and further discloses each arbiter circuit implements an independent priority policy to route information to said plurality of graphics processing units (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 50, Kurihara teaches all the claimed subject matters as discussed in claim 49, and further discloses said priority policy is a static policy (Kurihara, Fig. 1, col. 3, lines 5-40).

As per claim 51, Kurihara teaches all the claimed subject matters as discussed in claim 49, except for explicitly disclosing priority policy is a least recently used policy. However, Kurihara discloses selecting a processing unit have sufficient space (Kurihara, Fig. 1, col. 3, lines 5-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to route information to graphics processing units using least recently used policy in order to reduce waiting time. Therefore, it would have been obvious to one of ordinary skill in the art

at the time the invention was made to route information to graphics processing units using least recently used policy in order to reduce waiting time.

As per claim 52, Kurihara teaches all the claimed subject matters as discussed in claim 49, except for explicitly disclosing priority policy is a round-robin policy. However, Kurihara discloses selecting a processing unit have sufficient space (Kurihara, Fig. 1, col. 3, lines 5-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to route information to graphics processing units using round-robin policy in order to reduce waiting time. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to route information to graphics processing units using round-robin policy in order to reduce waiting time.

As per claim 53, Kurihara teaches all the claimed subject matters as discussed in claim 49, except for explicitly disclosing priority policy is a fixed priority policy. However, Kurihara discloses selecting a processing unit have sufficient space (Kurihara, Fig. 1, col. 3, lines 5-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to route information to graphics processing units using a fixed priority policy in order to reduce waiting time. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to route information to graphics processing units using a fixed priority policy in order to reduce waiting time.

As per claim 54, Kurihara teaches all the claimed subject matters as discussed in claim 49, except for explicitly disclosing priority policy is a dynamic priority policy. However, Kurihara discloses selecting a processing unit have sufficient space (Kurihara, Fig. 1, col. 3, lines 5-40). It would have been obvious to one of ordinary skill in the art at the time the invention was

made to route information to graphics processing units using a dynamic priority policy in order to reduce waiting time. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to route information to graphics processing units using a dynamic priority policy in order to reduce waiting time.

Claims 55-67 are rejected on grounds corresponding to the reasons given above for claims 32-54.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Morozumi (6,570,571) discloses image processing apparatus and method for efficient distribution of image processing to plurality of graphics processors.

Aleksic et al. (6,469,703) disclose system of accessing data in a gr5aphics system and method thereof.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chongshan Chen whose telephone number is (703) 305-8319. The examiner can normally be reached on Monday - Friday (8:00 am - 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y Vu can be reached on (703)305-4393. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

CC
June 13, 2003

KIM VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100